CLAIMS:

1. A semiconductor processing method comprising:

forming first and second layers over a substrate, the second layer having a higher oxidation rate than the first layer when exposed to an oxidizing atmosphere, the substrate having a periphery, the first layer having an exposed first outer edge spaced inside the substrate periphery, the second layer having an exposed first outer edge spaced inside the substrate periphery;

etching into the second layer first edge at a faster rate than any etching into the first layer first edge and forming an exposed second outer edge of the second layer; and

after the etching, exposing the substrate to the oxidizing atmosphere with the second layer second outer edge exposed and forming an oxidized first layer edge.

2. The method of claim 1 comprising forming the second layer over the first layer. - -

3. The method of claim 1 comprising forming the first layer over the second layer.

4. The method of claim 1 comprising forming the first and second layers to be electrically conductive.

5. The method of claim 1 wherein the etching comprises wet etching.

6. The method of claim 1 wherein the etching comprises wet etching with a basic solution.

7. The method of claim 1 wherein the etching comprises wet etching with a solution comprising ammonium hydroxide and hydrogen peroxide.

8. The method of claim 1 further comprising forming a third layer over the first and second layers, the third layer having an exposed first outer edge spaced inside the substrate periphery, the third layer having a lower oxidation rate than the oxidation rate of the second layer when exposed to the oxidizing atmosphere, the etching into the second layer first edge forming the second layer second edge to be recessed inwardly relative to outer edges of both the first and third layers.

9. A semiconductor processing method comprising:

forming a stack of at least two conductive layers for an electronic component over a substrate, the two conductive layers having different oxidation rates when exposed to an oxidizing atmosphere, the layer with the higher oxidation rate having an outer lateral edge which is recessed inwardly of a corresponding outer lateral edge of the layer with the lower oxidation rate; and

exposing the stack of conductive layers to the oxidizing atmosphere effective to grow an oxide layer over the outer lateral edges of the first and second layers.

10. The method of claim 9 comprising forming the higher oxidation rate layer over the lower oxidation rate layer.

11. The method of claim 9 comprising forming the lower oxidation rate layer over the higher oxidation rate layer.

12. The method of claim 9 comprising forming another layer over the at least two conductive layers, the another layer having a lower oxidation rate than the layer having said higher oxidation rate when exposed to the oxidizing atmosphere, the outer lateral edge of the layer with said higher oxidation rate being recessed inwardly of a corresponding outer lateral edge of the another layer.

13. The method of claim 12 wherein the another layer is electrically insulative.

14. The method of claim 9 wherein one of the at least two conductive layers comprises conductively doped polysilicon and another of the at least two conductive layers comprises a refractory metal silicide.

15. A method of forming an electronic component comprising:

forming first and second conductive materials over a substrate, the second material having a higher oxidation rate than an oxidation rate of the first material when exposed to an oxidizing atmosphere;

first etching the first and second conductive materials to form a conductive component, the conductive component having opposing substantially continuous straight linear outer lateral edges of the first and second conductive materials;

second etching into the second material outer lateral edges to recess them inside of the first material outer lateral edges; and

after the second etching, exposing the substrate to the oxidizing atmosphere effective to grow an oxide layer over the outer lateral edges of the first and second conductive materials.

16. The method of claim 15 one of the first and second conductive materials comprises conductively doped polysilicon and the other comprises a refractory metal silicide.

17. The method of claim 15 wherein the second etching comprises wet etching.

18. The method of claim 15 wherein the first etching comprises dry etching and the second etching comprises wet etching.

19. The method of claim 15 wherein the second etching comprises wet etching with a basic solution.

20. The method of claim 15 wherein the second etching comprises wet etching with a solution comprising ammonium hydroxide and hydrogen peroxide.

21. The method of claim 15 comprising forming the second conductive material to be received over the first conductive material.

22. The method of claim 15 wherein the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another.

23. The method of claim 15 wherein the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another, and further comprising ion implanting into the substrate proximate outer lateral edges of the first and the second conductive materials after the exposing.

24. The method of claim 15 wherein the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another, the second etching and the exposing being effective to form the oxide layer to have opposing substantially continuous straight linear outer lateral edges over the first and second conductive materials.

25. The method of claim 24 wherein the opposing linear outer lateral edges of the oxide layer are formed to be less than 1 micron apart.

- -

26. The method of claim 15 comprising forming a third insulative material over the first and second conductive materials, the first etching also etching the third insulative material to form the conductive component to have an insulative cap, the third insulative material having a lower oxidation rate than the second conductive material when exposed to the oxidizing atmosphere, the second etching recessing the second material outer lateral edges to within outer lateral edges of the third insulative material.

27. The method of claim 26 wherein the first etching is conducted to form the insulative cap to have opposing outer lateral edges which are substantially straight continuously linear with the outer lateral edges of the first and second conductive materials, and the first etching is conducted to space said opposing linear outer lateral edges less than 1 micron apart from one another.

28. The method of claim 26 wherein the first etching is conducted to form the insulative cap to have opposing outer lateral edges which are substantially straight continuously linear with the outer lateral edges of the first and second conductive materials, and the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another, and further comprising ion implanting into the substrate proximate outer lateral edges of the first and the second conductive materials after the exposing.

29. The method of claim 26 wherein the first etching is conducted to form the insulative cap to have opposing outer lateral edges which are substantially straight continuously linear with the outer lateral edges of the first and second conductive materials, and the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another, the second etching and the exposing being effective to form the oxide layer to have opposing substantially continuous-straight linear outer lateral edges over the first and second conductive materials.

30. The method of claim 29 wherein the opposing linear outer lateral edges of the oxide layer are formed to be less than 1 micron apart.

31. A semiconductor processing method of forming a transistor comprising:

forming a gate dielectric layer, a doped silicon layer, a silicide layer and an insulating layer over a channel region of a substrate, the silicide layer having a higher oxidation rate than oxidation rates of the doped silicon layer and the insulating layer when exposed to an oxidizing atmosphere;

first etching the insulating layer, the silicide layer and the doped silicon layer to form a conductive gate stack having an insulating cap over the channel region, the gate stack having two opposing and respectively linearly aligned outer lateral edges of the insulating, silicide and doped silicon layers;

second etching the silicide layer substantially selectively relative to the insulating cap and the doped silicon layer to recess outer lateral edges of the silicide layer to within outer lateral edges of both the insulating and doped silicon layers of the gate stack;

after the second etching, exposing the substrate to the oxidizing atmosphere effective to grow an oxide layer over outer lateral edges of the silicide and doped silicon layers;

after the exposing, first implanting a dopant impurity into the substrate proximate the gate stack to form at least one of an LDD region or a halo region;

after the first implanting, forming insulative material over the oxide layer; and

after forming the insulative material, second implanting a dopant impurity into the substrate proximate the gate stack to form transistor source/drain regions.

32. The method of claim 31 wherein the first etching is conducted to space the opposing substantially linear outer lateral edges less than 1 micron apart from one another.

33. The method of claim 31 wherein the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another, the second etching and the exposing being effective to form the oxide layer to have opposing substantially continuous straight linear outer lateral edges over the insulating, silicide and doped silicon layers.

34. The method of claim 33 wherein the opposing linear outer lateral edges of the oxide layer are formed to be less than 1 micron apart.

35. The method of claim 31 wherein the second etching comprises wet etching.

36. The method of claim 31 wherein the first etching comprises dry etching and the second etching comprises wet etching.

37. The method of claim 31 wherein the second etching comprises wet etching with a basic solution.

38. The method of claim 31 wherein the second etching comprises wet etching with a solution comprising ammonium hydroxide and hydrogen peroxide.

39. A transistor comprising:

a semiconductive substrate;

a stack of a gate dielectric layer over the semiconductive substrate, a first conductive layer over the gate dielectric layer, a second conductive layer different in composition from the first and received over the first, and an insulative cap over the second conductive layer; the first conductive layer of the stack having opposing outer lateral edges which are spaced less than one micron apart defining a channel length within the semiconductive substrate of less than one micron, the second conductive layer of the gate stack having opposing outer lateral edges which are spaced apart less than the opposing outer lateral edges of the first conductive layer are spaced apart; and

an oxide layer formed over the outer lateral edges of the first conductive layer, the second conductive layer and the insulative cap, the oxide layer having opposing substantially continuous straight linear outer lateral edges over the insulating cap, the first conductive layer and the second conductive layer.

40. The transistor of claim 39 wherein the opposing linear outer lateral edges of the oxide layer are formed to be less than 1 micron apart.

41. The transistor of claim 39 wherein the oxide layer has a lateral thickness of less than 100 Angstroms over the first conductive layer.

42. The transistor of claim 39 wherein the oxide layer has a lateral thickness of less than 100 Angstroms and greater than 10 Angstroms over the first conductive layer.

43. A transistor comprising:

a semiconductive substrate;

a gate stack formed over the semiconductive substrate and defining in at least one cross section a channel length within the semiconductive substrate of less than 1 micron, the gate stack comprising conductive material formed over a gate dielectric layer; and

an insulative layer formed on outer lateral edges of the conductive material, the insulative layer having opposing substantially continuous straight linear outer lateral edges over all conductive material of the gate stack within the one cross section.

44. The transistor of claim 43 wherein the opposing linear outer lateral edges of the insulative layer are formed to be less than 1 micron apart.

45. The transistor of claim 43 wherein the insulative layer has a minimum lateral thickness of less than 100 Angstroms over said all conductive material.

46. The transistor of claim 43 wherein the insulative layer has a minimum lateral thickness of less than 100 Angstroms and greater than 10 Angstroms over said all conductive material.

47. The transistor of claim 43 wherein the conductive material comprises at least two conductive layers, the conductive layers within the one cross section of the gate stack having opposing outer lateral edges which are displaced from one another.